Notice of Allowability	Application No.	Applicant(s)	
	10/669,083	PICOLLET ET AL.	
	Examiner	Art Unit	
	Stephen J. Cherry	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7-24-2006*.

2. ☒ The allowed claim(s) is/are *1,2,9,10,17-40*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Taylor on 6-5-2006.

The application has been amended as follows:

Delete claim 1 and replace with:

1. Method of estimating an electrical capacitance of a circuit component comprising:

a first rectangular conducting plate, having a width W, a length L and a thickness t_{M1};

a second conducting plate, parallel to the first plate and separated from the latter by a distance t_{Ox}, having a rectangular central part facing the first plate and a peripheral part surrounding said central part;

a first homogeneous dielectric, of relative dielectric permittivity ε_{Ox}, placed between the first and second plates and having a thickness of t_{Ox} between the two plates and of t_{OxSt} in line with said peripheral part of the second plate, so that said first dielectric has a height step $t_{Ox} - t_{OxSt}$ around the perimeter of the first plate; and

a second homogeneous dielectric, of relative dielectric permittivity ε_E, surrounding the first plate and the first dielectric,

the method comprising:

calculating a sum of several terms including at least two terms of the form $C_0.W.L$ and $C_1.2(W+L)$, with $C_0 = \frac{\varepsilon_0 \cdot \varepsilon_{Ox}}{t_{Ox}}$ and $C_1 = \frac{\varepsilon_0}{\pi} \cdot K \cdot Ln(a)$,

- ε_0 being the dielectric permittivity of free space,
- $K = \frac{\varepsilon_{Ox} \cdot \varepsilon_E}{\varepsilon_{Ox} - \left(\frac{(\varepsilon_E - \varepsilon_{Ox})^2}{(\varepsilon_E + \varepsilon_{Ox})} \cdot \frac{t_{OxSt}}{t_{Ox}} \right)}$,
- $a = -1 + 2k^2 + 2k\sqrt{k^2 - 1}$ with $k = 1 + \frac{t_{M1}}{t_{Ox}}$; and

storing the calculated sum as an estimated capacitance of the component.

Delete claim 9 and replace with:

9. Method of determining a dimension of a capacitor of electrical capacitance C_u comprising:

a first rectangular conducting plate, having a width W, a length L and a thickness t_{M1};

a second conducting plate, parallel to the first plate and separated from the latter by a distance t_{Ox}, having a rectangular central part facing the first plate and a peripheral part surrounding said central part;

a first homogeneous dielectric, of relative dielectric permittivity ε_{Ox}, placed between the first and second plates and having a thickness of t_{Ox} between the two plates and of t_{OxSt} in line with said peripheral part of the second plate, so that said first dielectric has a height step $t_{Ox} - t_{OxSt}$ around the perimeter of the first plate; and

a second homogeneous dielectric, of relative dielectric permittivity ε_E, surrounding the first plate and the first dielectric,

the method comprising:

calculating a sum of first terms including C_u and at least one term of the form $-2 \cdot C_1 \cdot W$ divided by a sum of second terms including at least two terms of the form $C_0.W$ and $2.C_1$, with $C_0 = \frac{\varepsilon_0 \cdot \varepsilon_{Ox}}{t_{Ox}}$ and $C_1 = \frac{\varepsilon_0}{\pi}.K.\ln(a)$,

- ε_0 being the dielectric permittivity of free space,
- $K = \dfrac{\varepsilon_{Ox} \cdot \varepsilon_E}{\varepsilon_{Ox} - \left(\dfrac{(\varepsilon_E - \varepsilon_{Ox})^2}{(\varepsilon_E + \varepsilon_{Ox})} \cdot \dfrac{t_{OxSt}}{t_{Ox}} \right)}$,
- $a = -1 + 2k^2 + 2k\sqrt{k^2 - 1}$ with $k = 1 + \dfrac{t_{M1}}{t_{Ox}}$; and

storing the calculated sum as a first approximate value L_1 of the length L.

Delete claim 17 and replace with:

17. A method of estimating an electrical capacitance of a circuit component comprising,

a rectangular first conducting plate,

a second conducting plate parallel to the first plate, having a rectangular central part facing the first plate and a peripheral part surrounding said central part,

a first homogeneous dielectric placed between the first and second conducting plates, and

a second homogeneous dielectric surrounding the first conducting plate and the first dielectric,

the method comprising the steps of:

estimating a capacitance of a first partial capacitor formed by the lower surface of the first conducting plate and the central part of the upper surface of the second conducting plate;

estimating a capacitance of a second partial capacitor formed by the sides of the first conducting plate and the peripheral part of the upper surface of the second conducting plate;

summing the estimated capacitances of the first and second partial capacitors; and

storing the sum as an estimated capacitance of the circuit component.

Delete claim 26 and replace with:

26. A method of estimating a dimension of a capacitor having a desired electrical capacitance, the capacitor comprising,

a rectangular first conducting plate, having a width,

a second conducting plate parallel to the first plate, having a rectangular central part facing the first plate and a peripheral part surrounding said central part,

a first homogeneous dielectric placed between the first and second conducting plates, and

a second homogeneous dielectric surrounding the first conducting plate and the first dielectric,

the method comprising the steps of:

estimating a capacitance per unit of area of a first partial capacitor formed by the lower surface of the first conducting plate and the central part of the upper surface of the second conducting plate;

estimating a capacitance per unit of length of a second partial capacitor formed by the sides of the first conducting plate and the peripheral part of the upper surface of the second conducting plate;

calculating a function of the desired electrical capacitance, the estimated capacitance per unit of area of the first capacitor, the estimated capacitance per unit of length of the second partial capacitor, and the width of the first conducting plate; and

storing a result of the calculated function as an estimated length of the first conducting plate.

Delete claim 35 and replace with:

35. A method of simulating the electrical behavior of an electronic circuit comprising a circuit component, the circuit component comprising

a first rectangular conducting plate,

a second conducting plate parallel to the first plate, having a rectangular central part facing the first conducting plate and a peripheral part surrounding said central part,

a first homogeneous dielectric placed between the first and second conducting plates, and

a second homogeneous dielectric surrounding the first conducting plate and the first dielectric,

the method comprising the steps of:

estimating a capacitance of a first partial capacitor formed by the lower surface of the first conducting plate and the central part of the upper surface of the second conducting plate;

estimating a capacitance of a second partial capacitor formed by the sides of the first conducting plate and the peripheral part of the upper surface of the second conducting plate;

summing the estimated capacitances of the first and second partial capacitors; and

storing the sum as an estimated capacitance of the circuit component.

Claims 1-2, 9-10, 17-40 are allowed.

The following is an examiner's statement of reasons for allowance:

Claim 1 recites, "calculating a sum of several terms including at least two terms of the form $C_0.W.L$ and $C_1.2(W+L)$, with $C_0 = \frac{\varepsilon_0 \cdot \varepsilon_{Ox}}{t_{Ox}}$ and $C_1 = \frac{\varepsilon_0}{\pi} \cdot K \cdot Ln(a)$,

- ε_0 being the dielectric permittivity of free space,
- $K = \frac{\varepsilon_{Ox} \cdot \varepsilon_E}{\varepsilon_{Ox} - \left(\frac{(\varepsilon_E - \varepsilon_{Ox})^2}{(\varepsilon_E + \varepsilon_{Ox})} \cdot \frac{t_{OxSt}}{t_{Ox}} \right)}$,
- $a = -1 + 2k^2 + 2k\sqrt{k^2 - 1}$ with $k = 1 + \frac{t_{M1}}{t_{Ox}}$; and

storing the calculated sum as an estimated capacitance of the component" with claimed dielectric sturcture. This feature, in combination with additional claimed structure, overcomes the prior art of record.

Claim 9 recites, "calculating a sum of first terms including C_u and at least one term of the form $-2 \cdot C_1 \cdot W$ divided by a sum of second terms including at least two terms of the form $C_0.W$ and $2.C_1$, with $C_0 = \frac{\varepsilon_0 \cdot \varepsilon_{Ox}}{t_{Ox}}$ and $C_1 = \frac{\varepsilon_0}{\pi}.K.ln(a)$,

- ε_0 being the dielectric permittivity of free space,
- $K = \frac{\varepsilon_{Ox} \cdot \varepsilon_E}{\varepsilon_{Ox} - \left(\frac{(\varepsilon_E - \varepsilon_{Ox})^2}{(\varepsilon_E + \varepsilon_{Ox})} \cdot \frac{t_{OxSt}}{t_{Ox}} \right)}$,
- $a = -1 + 2k^2 + 2k\sqrt{k^2 - 1}$ with $k = 1 + \frac{t_{M1}}{t_{Ox}}$; and

storing the calculated sum as a first approximate value L_1 of the length L" with claimed dielectric sturcture. This feature, in combination with additional claimed structure, overcomes the prior art of record.

Claim 17 recites, "estimating a capacitance of a second partial capacitor formed by the sides of the first conducting plate and the peripheral part of the upper surface of the second conducting plate; summing the estimated capacitances of the first and second partial capacitors; and storing the sum as an estimated capacitance of the circuit component", with claimed dielectric sturcture. This feature, in combination with additional claimed structure, overcomes the prior art of record.

Claim 26 recites, "estimating a capacitance per unit of length of a second partial capacitor formed by the sides of the first conducting plate and the peripheral part of the upper surface of the second conducting plate; calculating a function of the desired electrical capacitance, the estimated capacitance per unit of area of the first capacitor, the estimated capacitance per unit of length of the second partial capacitor, and the width of the first conducting plate; and storing a result of the calculated function as an estimated length of the first conducting plate" with claimed dielectric sturcture. This feature, in combination with additional claimed structure, overcomes the prior art of record.

Claim 35 recites, "estimating a capacitance of a second partial capacitor formed by the sides of the first conducting plate and the peripheral part of the upper surface of the second conducting plate; summing the estimated capacitances of the first and second partial capacitors; and storing the sum as an estimated capacitance of the

circuit component" with claimed dielectric sturcture. This feature, in combination with additional claimed structure, overcomes the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen J. Cherry whose telephone number is (571) 272-2272. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJC

John Barlow
Supervisory Patent Examiner
Technology Center 2800